UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,664	05/24/2007	Spartak Gevorgian	0110-094	9040

42015 7590 11/07/2008

POTOMAC PATENT GROUP PLLC
P. O. BOX 270
FREDERICKSBURG, VA 22404

EXAMINER	
SINCLAIR, DAVID M	

ART UNIT	PAPER NUMBER
2831	

NOTIFICATION DATE	DELIVERY MODE
11/07/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/596,664	GEVORGIAN ET AL.	
	Examiner	Art Unit	
	DAVID M. SINCLAIR	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/25/2007 & 01/18/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "110" has been used to designate both first plate and first ordinary metal layer. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 30-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda et al. (6,465,832).

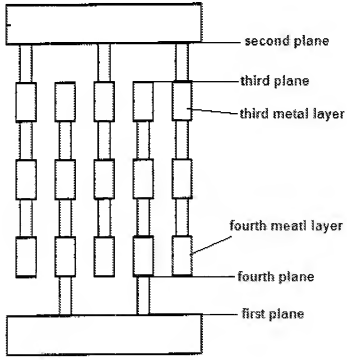

Figure 1: Altered version of Maeda '832 fig. 25 showing examiner labels

In regards to claim 30, Maeda '832 discloses

A method of arranging an on-chip capacitor on a chip to create a capacitance between a first conducting connection point (7b – fig. 25; column 8 – line 58 to column 9 – line 6) in a first plane (present office action fig. 1 (POA1)) of the chip and a second conducting connection point (7a – fig. 25; column 8 – line 58 to column 9 – line 6) in a second plane (POA1) of the chip, comprising the steps of creating at least one conducting extension of a first type (9 & 3b – fig. 25; column 8 – line 58 to column 9 – line 6) from the first conducting connection point toward the second plane to a third plane (POA1), and creating at least one conducting extension of a second type (6 & 3a – fig. 25; column 8 – line 58 to column 9 – line 6) from the second conducting connection point toward the first plane to a fourth plane (POA1), wherein the fourth plane is located between the first plane and the second plane, the third plane is located between the fourth plane and the second plane (POA1), and the conducting extension of the first type is isolated from the conducting extension of the second type by a dielectric (2 – fig. 25; column 8 – line 58 to column 9 – line 6) allowing an electric field to be created between the conducting extensions.

In regards to claim 31, Maeda '832 discloses

The method of claim 30, wherein a plurality of conducting extensions of the first type are created (fig. 25).

In regards to claim 32, Maeda '832 discloses

The method of claim 30, wherein a plurality of conducting extensions of the second type are created (fig. 25).

In regards to claim 33, Maeda '832 discloses

The method of claim 30, wherein the first plane is a side of a first metal layer, the second plane is a side of a second metal layer, and the first and second metal layers are different metal layers (column 8 – line 19; POA1).

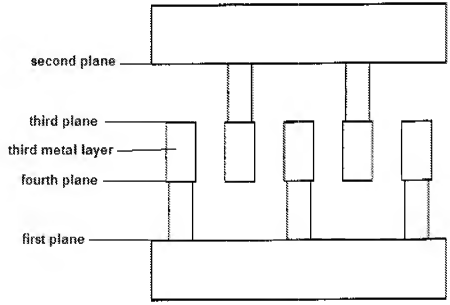

Figure 2: Altered version of Maeda '832 fig. 21 with examiner labels

In regards to claim 34, Maeda '832 discloses

The method of claim 33, wherein the third and fourth planes are different sides of a third metal layer (POA2).

In regards to claim 35, Maeda '832 discloses

The method of claim 33, wherein the third plane is a side of a third metal layer, the fourth plane is a side of a fourth metal layer, and the third and fourth metal layers are different metal layers (POA1).

In regards to claim 36, Maeda '832 discloses

The method of claim 30, wherein the at least one conducting extension of the first type originates in a metal layer and terminates in a metal layer (POA1).

In regards to claim 37, Maeda '832 discloses

The method of claim 36, wherein the at least one conducting extension of the first type extends through at least one further metal layer (POA1).

In regards to claim 38, Maeda '832 discloses

The method of claim 30, wherein the at least one conducting extension of the second type originates in a metal layer and terminates in a metal layer (POA1).

In regards to claim 39, Maeda '832 discloses

The method of claim 38, wherein the at least one conducting extension of the second type extends through at least one further metal layer (POA1).

In regards to claim 40, Maeda '832 discloses

The method of claim 30, further comprising the step of extending the first conducting connection point in the first plane of the chip such that the first conducting connection point comprises a conducting plate (fig. 25).

In regards to claim 41, Maeda '832 discloses

The method of claim 30, further comprising the step of extending the second conducting connection point in the second plane of the chip such that the second conducting connection point comprises a conducting plate (fig. 25).

In regards to claim 42, Maeda '832 discloses

The method of claim 30, further comprising the step of arranging one or more on-chip capacitors with at least one other passive component into an on-chip resonant circuit (fig. 36; column 10 – line 64 to column 11 – line 15).

In regards to claim 43, Maeda '832 discloses

The method of claim 30, further comprising the step of arranging one or more on-chip capacitors into an on-chip transmission line (fig. 25; capacitor structure is a transmission line).

In regards to claim 44, Maeda '832 discloses

An on-chip capacitor with a capacitance between a first conducting connection point (7b – fig. 25; column 8 – line 58 to column 9 – line 6) in a first plane (present office action fig. 1 (POA1)) of the chip and a second conducting connection point (7a – fig. 25; column 8 – line 58 to column 9 – line 6) in a second plane (POA1) of the chip, the on-chip capacitor comprising: at least one conducting extension of a first type (9 & 3b – fig. 25; column 8 – line 58 to column 9 – line 6) from the first conducting connection point toward the second plane to a third plane (POA1), and at least one conducting extension of a second type (6 & 3a – fig. 25; column 8 – line 58 to column 9 – line 6) from the second conducting connection point toward the first plane to a fourth plane (POA1), wherein the fourth plane is located between the first plane and the second plane, the third plane is located between the fourth plane and the second plane (POA1), and the conducting extension of the first type is isolated from the conducting extension of the second type by a dielectric (2 – fig. 25; column 8 – line 58 to column 9 – line 6) allowing an electric field to be created between the conducting extensions.

In regards to claim 45, Maeda '832 discloses

The on-chip capacitor of claim 44, wherein the on-chip capacitor comprises a plurality of conducting extensions of the first type (fig. 25).

In regards to claim 46, Maeda '832 discloses

The on-chip capacitor of claim 44, wherein the on-chip capacitor comprises a plurality of conducting extensions of the second type (fig. 25).

In regards to claim 47, Maeda '832 discloses

The on-chip capacitor of claim 44, wherein the first plane is a side of a first metal layer, the second plane is a side of a second metal layer, and the first and second metal layers are different metal layers (column 8 – line 19; POA1).

In regards to claim 48, Maeda '832 discloses

The on-chip capacitor of claim 47, wherein the third and fourth planes are different sides of a third metal layer (POA2).

In regards to claim 49, Maeda '832 discloses

The on-chip capacitor of claim 47, wherein the third plane is a side of a third metal layer, the fourth plane is a side of a fourth metal layer, and the third and the fourth metal layers are different metal layers (POA1).

In regards to claim 50, Maeda '832 discloses

The on-chip capacitor of claim 44, wherein the at least one conducting extension of the first type originates in a metal layer and terminates in a metal layer (POA1).

In regards to claim 51, Maeda '832 discloses
The on-chip capacitor of claim 50, wherein the at least one conducting extension of the first type extends through at least one further metal layer (POA1).

In regards to claim 52, Maeda '832 discloses
The on-chip capacitor of claim 44, wherein the at least one conducting extension of the second type originates in a metal layer and terminates in a metal layer (POA1).

In regards to claim 53, Maeda '832 discloses
The on-chip capacitor of claim 52, wherein the at least one conducting extension of the second type extends through at least one further metal layer (POA1).

In regards to claim 54, Maeda '832 discloses
The on-chip capacitor of claim 44, wherein the first conducting connection point in the first plane of the chip comprises a conducting plate (fig. 25).

In regards to claim 55, Maeda '832 discloses

The on-chip capacitor of claim 44, wherein the second conducting connection point in the second plane of the chip comprises a conducting plate (fig. 25).

In regards to claim 56, Maeda '832 discloses

The on-chip capacitor of claim 44, wherein the on-chip capacitor is included in a resonant circuit (fig. 36; column 10 – line 64 to column 11 – line 15).

In regards to claim 57, Maeda '832 discloses

An on-chip transmission line, wherein the transmission line comprises at least one on-chip capacitor defined by claim 44 (fig. 25; capacitor structure is a transmission line).

In regards to claim 58, Maeda '832 discloses

The on-chip transmission line of claim 57, wherein the on-chip transmission line is included in a resonator, matching network, or power splitter (fig. 36; column 10 – line 64 to column 11 – line 15).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

USPGPUB 2003/0234415 – fig. 3

USPAT 6,570,210 – fig. 6

USPAT 6,635,916

USPAT 6,737,698 – fig. 8

USPAT 6,864,526 – figs. 4, 7, 12

USPAT 6,037,621 – figs. 3, 7, & 8

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID M. SINCLAIR whose telephone number is (571)270-5068. The examiner can normally be reached on Mon - Thurs. 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F. Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Diego Gutierrez/
Supervisory Patent Examiner, Art Unit 2831

/D. M. S./
Examiner, Art Unit 2831